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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/532,292	04/21/2005	Franciscus Petrus Widdershoven	BE02 0032 US	8750

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EXAMINER	
TAYLOR, EARL N	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 10/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EV

Office Action Summary	Application No.	Applicant(s)	
	10/532,292	WIDDERSHOVEN ET AL.	
	Examiner	Art Unit	
	Earl N. Taylor	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6* is/are allowed.

6)☒ Claim(s) *7-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Objection:

Regarding the Transmittal Letter to the United States Designated/Elected Office (DO/EO/US) Concerning a Filing Under 35 U.S.C. 371. The international filing date of 18 August 2002 appears to be in error and should be 18 August 2003 as cited on the published PCT and as stated in the Oath and Declaration of the instant application.

Specification

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 9, 10, 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Claim 9 recites the limitation "said second self-aligned silicide area" and "said contact opening" in lines 5 and 6. There is insufficient antecedent basis for this limitation in the claim. Claims 10, 13 and 14 include the limitations of Claim 9.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 7, 8, 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma et al. (U.S. Patent 5,364,806).**

Referring to Claim 7, Ma teaches, in Fig. 2A-3, a memory cell, for storing at least one bit, on a semiconductor substrate (26), comprising on said substrate a first floating gate stack (22), a second floating gate stack (20) and an intermediate access gate (select gate; 24A), said first and second floating gate stacks (22 and 20) comprising a first gate oxide layer (22D and 20D), a floating gate (22B and 20B), a control gate (22C and 20C), an interpoly dielectric layer (22E and 20E), a capping layer (22F and 20F) and sidewall spacers (Col. 5, Lines 66-68), said first gate oxide layer (22D and 20D) being located on said substrate (26), said floating gate (22B and 20B) being on top of said first gate oxide layer (22D and 20D), said interpoly dielectric layer (22E and 20E) being on top of said floating gate (22B and 20B), said control gate (22C and 20C) being on top of said interpoly dielectric layer (22E and 20E), said capping layer (22F and 20F) being on top of said control gate (22C and 20C), said memory cell further comprising source and drain contacts (22A and 20A), characterized in that said first and second floating gate stacks (22 and 20) have substantially equal heights; said intermediate access gate (24A) comprises a poly-Si layer (Abstract) in between said first and second floating gate stacks (22 and 20). The language, term, or phrase "planarized poly-Si layer", is directed towards the process of planarizing. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In*

re Avery, 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language "planarized poly-Si layer" only requires a poly-Si layer, which does not distinguish the invention from Ma, who teaches the structure as claimed.

Referring to Claim 8, Ma teaches all of the limitations of Claim 7 wherein an array of memory cells, characterized in that said array comprises at least two adjacent memory cells as shown in Fig. 3.

Referring to Claim 11, Ma teaches all of the limitations of Claims 7 and 8 whereing said at least two memory cells are programmed selectively, and said at least two memory cells are erased by Fowler-Nordheim Tunneling. It has been held that when the claimed and prior art products are identical in structure or composition, a prima facie case of either anticipation or obviousness has been established. See MPEP § 2112.01. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997).

Referring to Claim 12, Ma teaches all of the limitations of Claims 7 and 8 wherein said at least two memory cells are programmed selectively and said at least two memory cells are erased by Fowler-Nordheim Tunneling (Col. 6, Lines 18-47). It has been held that when the claimed and prior art products are identical in structure or composition, a prima facie case of either anticipation or obviousness has been established. See MPEP § 2112.01. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997).

Referring to Claim 15, Ma teaches all of the limitations of Claim 7 wherein a semiconductor device comprises at least one said memory cell.

Allowable Subject Matter

5. Claims 9, 10, 13 and 14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 9, the prior art of record alone or in combination neither teaches nor makes obvious the invention wherein a bit-line is a metal line; said bit-line being connected to a self-aligned silicide area by a contact in a contact opening in combination with all of the limitations of Claims 7, 8 and 9.

Claims 1-6 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding Claim 1, the prior art of record alone or in combination neither teaches nor makes obvious the invention wherein said poly-Si layer being deposited in between said first and second floating gate stacks in a thickness equal to or larger than the height of said first and second floating gate stacks, planarizing said poly-Si layer by chemical mechanical polishing to obtain a planarized poly-Si layer, using said capping layer of said first and second floating gate stacks as a polish stop layer; defining said intermediate access gate in said planarized poly-Si layer by a masking step with an access gate mask over said planarized poly-Si layer between said first and second floating gate stacks and an etching step for poly-Si in combination with all of the limitations of Claim 1. Claims 2-6 include the limitations of Claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

Primary Examiner